CLAIMS

What is claimed is:

1. A method of manufacturing an integrated circuit (IC) device having a given layout, said method comprising:

simulating how structures within the layout will pattern on a wafer for a plurality of resolution enhancement techniques (RETs);

evaluating manufacturability of structures within each simulation; and

selecting one or more RETs that provide optimal manufacturability.

2. The method of claim 1, wherein the evaluating step includes:

performing optical rule checking (ORC) on structures within each simulation; and

for each simulation, calculating a percentage of optically different edges that demonstrate acceptable manufacturability.

3. The method of claim 2, wherein the selecting step includes:

selecting RETs that correspond to simulations having a percentage of acceptable optically different edges that is greater than a predefined value.

4. The method of claim 1, wherein each RET includes a combination of illuminator parameters, numerical aperture (NA) and mask parameters.

5. The method of claim 4, wherein the illuminator parameters include at least one of (i) illuminator source shape, (ii) number of poles, (iii) orientation of poles, (iv) inner radius, (v) outer radius, and (vi) wedge angle.

6. The method of claim 4, wherein the mask parameters include at least one of mask type and mask transmission.

7. The method of claim 1, wherein the simulating step includes simulating variations over a predetermined range in at least one of focus, exposure and the mask.

8. The method of claim 2, wherein performing ORC includes checking structures within the simulations based on one of aerial image metrics, resist image metrics, and post exposure bake metrics.

9. The method of claim 8, wherein the aerial image metrics include at least one of image edge slope, image edge log slope, contrast, minimum intensity, maximum intensity, edge placement error and intensity at a given distance.

10. The method of claim 9, said method further comprising:

recording values for at least one of the metrics in a searchable data table structure.

11. The method of claim 1, said method further comprising:

based on the simulating step, providing a graphical representation indicating the manufacturability of the layout for the plurality of RETs.

12. The method of claim 4, said method further comprising:

exposing a wafer to an illumination source having selected illuminator parameters, said illumination source transmitting light energy through a mask having a pattern corresponding to the layout, said mask having selected mask parameters, the exposing being limited by a selected numerical aperture (NA);

wherein the selected illuminator parameters, mask parameters and NA correspond to one of the selected RETs.

13. An IC device manufactured according to the method of claim 12.

14. The method of claim 1, wherein the simulating step includes simulating and performing optical proximity correction (OPC) on the layout.

15. The method of claim 14, wherein simulating how structures within the layout will pattern for a plurality of RETs is performed using the same simulation engine as is used to perform OPC on the layout.

16. The method of claim 15, wherein the simulating step is automated with respect to performing OPC on the layout.

17. In a photolithography processing system having an associated numerical aperture (NA) value in which a reticle having a set of reticle parameters is exposed to an illuminator having a set of illuminator parameters to pattern a wafer with a desired layout, said method comprising:

simulating how the desired layout will pattern on a wafer for a plurality of combinations of different NA values, illuminator parameters and reticle parameters;

for each combination of NA values, illuminator parameters and reticle parameters, classifying structures within the associated simulated layouts based on manufacturability; and

selecting at least one combination of NA value, illuminator parameters and reticle parameters based on the classifying step.

18. The method of claim 17, wherein the classifying step includes:

performing optical rule checking (ORC) on structures within each simulation; and

for each simulation, calculating a percentage of optically different edges that demonstrate acceptable manufacturability.

19. The method of claim 18, wherein performing ORC includes checking structures within the simulations based on one of aerial image metrics, resist image metrics, and post exposure bake metrics.

20. The method of claim 17, wherein the illuminator parameters include at least one of (i) illuminator source shape, (ii) number of poles, (iii) orientation of poles, (iv) inner radius, (v) outer radius, and (vi) wedge angle.

21. The method of claim 17, wherein the simulating step is performed automatically using the same simulation engine as is used for performing optical proximity correction (OPC) and mask data preparation.

22. A method of minimizing wafer critical dimension (CD) variation in an integrated circuit (IC) device wafer patterned with a desired layout, said method comprising:

simulating how the desired layout will print on the wafer for a plurality of RET process windows, each RET process window corresponding to a plurality of lithography process parameters;

for each RET process window, classifying edges of structures within the simulated layout based on manufacturability; and

selecting one or more RET process windows that provide optimal manufacturability.

23. The method of claim 22, wherein the simulating step includes simulating at least one of focus variations, exposure variations and the mask variations.

24. The method of claim 23, wherein the classifying step includes:

performing optical rule checking (ORC) on edges of structures within each simulation; and

for each simulation, calculating a percentage of optically different edges that demonstrate acceptable manufacturability.